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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,560	GUO	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-26,35 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6, 9 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoll et al. (US 4,925,156) in view of Yoshimura (US 6,019,461).

With regard to Claim 1, Stoll et al., in Figure 5, discloses a circuit for driving a coil-armature device (10), comprising: a first switch which generates a switching signal configured to selectively activate the circuit (column 4 lines 9-12); a pulse width modulation signal generator (53); a second switch (27), responsive to said pulse width modulation signal generator, that causes a driving voltage source to periodically energize the coil-armature device according to a duty cycle; and a means (52) for selectively providing a signal from said pulse width modulation signal generator to said second switch after a determined time has elapsed after activation of the circuit (column 1 lines 13-20).

The first switch is not shown in Figure 5, however the first switch is coupled to terminals 11 & 12 (column 4 lines 9-12).

Stoll et al. does not teach that the signal generator includes an inverter and a feed-back loop configured to generate an input signal to said inverter based upon an output signal of the inverter.

Yoshimura et al., in Figure 2, teaches a signal generator comprising an inverter (22) and a feed-back loop (23) configured to generate an input signal to said inverter based upon an output signal of the inverter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stoll et al. with Yoshimura et al., by incorporating the signal generator of Yoshimura et al. in to the driving circuit of Stoll et al., for the purpose of providing a signal generator with few components thus providing a low cost.

With regard to Claim 2, Stoll et al. in view of Yoshimura et al., in Figure 2, discloses the circuit according to claim 1, wherein said elapsed time period corresponds to an amount of time required to sufficiently energize the coil armature device such that the armature is attracted into a center of the coil (column 4 lines 65-68 & column 5 lines 1-7).

With regard to Claim 3, Stoll et al. in view of Yoshimura et al., in Figure 2, discloses the circuit according to claim 1, wherein said elapsed time period corresponds to a time required to charge a capacitor (20) from a first charge level to a second charge level (column 4 lines 65-68 & column 5 lines 1-7).

With regard to Claim 4, Stoll et al, in Figure 2, discloses the circuit according to claim 1, wherein said means (38) for selectively providing a signal from said pulse width modulation signal generator (53) to said second switch (27) comprises a NAND gate responsive to a first input signal and said pulse width modulation signal (column 6 lines 25-54).

With regard to Claim 5, Stoll et al. in view of Yoshimura et al., in Figure 2, discloses the circuit of claim 4, wherein the first input signal to the NAND gate (38) is derived from a voltage level across a capacitor (20) (column 6 lines 25-54).

With regard to Claim 6, Stoll et al. in view of Yoshimura et al., in Figure 3, discloses the circuit according to claim 4, wherein said first input signal has a first voltage level upon activation of said circuit, and wherein said first input signal changes to a second voltage level after said determined time period has elapsed (Fig.3 U37).

With regard to Claim 9, Stoll et al. in view of Yoshimura et al. discloses the circuit of Claim 1. Yoshimura et a. further discloses that the input signal is dependant upon a voltage drop across a capacitor (27), said capacitor being periodically charged by said output signal of said inverter.

With regard to Claim 12, Stoll et al. in view of Yoshimura et al., in Figure 2, discloses the circuit according to claim 1, wherein said second switch (27) is a transistor.

2. Claims 7 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoll et al. in view of Yoshimura et al. as applied to claims 1 & 4 above, and further in view of Briedis et al. (US 5,510,951).

With regard to Claim 7, Stoll et al. in view of Yoshimura et al. teaches the circuit according to claim 4.

Stoll et al. in view of Yoshimura et al. does not teach that the pulse width modulation generator is configured to alternatively provide a first voltage level that is greater than an upper threshold voltage of said NAND gate and a second voltage level that is less than a lower threshold voltage of said NAND gate.

Briedis et al., in Figure 1, teaches an electronic control for 3-wire DC coils wherein a NAND gate (B) is used to change a solenoid (14) from a first energy level to a smaller energy level. When capacitor C1 becomes fully charged, NAND gate B is input to NAND gate A. Briedis et al. further teaches that the inputs of the NAND gates have Schmitt trigger characteristics (column 3 lines 28- 32) which is configured to alternatively provide a first voltage level that is greater than an upper threshold voltage of said NAND gate and a second voltage level that is less than a lower threshold voltage of said NAND gate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stoll et al. in view of Yoshimura et al. with Briedis et al., by using NAND gates with Schmitt triggers in the circuit by Stoll et al., for the purpose of providing noise immunity to the circuit when the input signal is near the thresholds.

With regard to Claim 10, Stoll et al. in view of Yoshimura et al. teaches the circuit of claim 1.

Stoll et al. in view of Yoshimura et al. does not teach that the inverter is a NAND gate configured as an inverter.

Briedis et al, in Figure 1, teaches that a NAND gate (B) can be configured as an inverter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stoll et al. in view of Yoshimura et al. with Briedis et al, by incorporating the NAND inverter into Stoll et al. in view of Yoshimura et al., for the purpose of providing a simple and cheap means of providing an inverter.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stoll et al. in view of Yoshimura et al. as applied to claim 1 above, and further in view of Hansen et al. (US 5,910,890).

With regard to Claim 11, Stoll et al. teaches the circuit according to claim 1.

Stoll et al. does not teach that the circuit further comprises a relay connected between said second switch and said means for selectively providing a signal from said pulse width modulation signal generator to said second switch.

Hansen et al., in Figure 2, teaches a transistor (Q3), which is an art recognized functional equivalent of a relay, connected between the second switch and the means for selectively providing a signal from the pulse width modulation signal generator to the second switch.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stoll et al. with Hansen et al., by providing a relay between the second switch a means for selectively providing a signal from the pulse width modulation signal generator taught by Stoll et al., for the purpose of providing a large amount of current to the base of transistor 27 in high current situations without damaging the NAND gate (38), and to use a relay instead of a transistor for the purpose of reducing the capacitance at the input of the NAND gate.

4. Claims 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen et al. (US 5,910,890) in view of Sasaki (JP 58005438).

With regard to Claim 13, Hansen et al., in Figure 2, discloses a circuit (30) for driving a coil-armature device (20, 21,22 & 24), comprising: a first switch, configured to selectively activate the circuit (column 2 lines 61-67); and a second switch (Q2),

responsive to a control signal, that causes a driving voltage source to periodically energize the coil-armature device according to one of a first duty cycle and a second duty cycle (column 1 lines 62-67 & column 2 lines 1-9).

Hansen et al. does not teach an analog switch, responsive to a change mode signal, that causes a transition from said first duty cycle to said second duty cycle.

Sasaki, in Figure 1, teaches an analog switch (S1), responsive to a change mode signal received from a comparator (4c).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hansen et al. with Sasaki, by incorporating the analog switch of Sasaki into the circuit of Hansen et al. by driving an analog switch with the comparator (56) wherein the switch is responsive to the change mode signal, that causes a transition from said first duty cycle to said second duty cycle, for the purpose of driving the diode (D7) with a switch instead of the current through the comparator thus preventing the comparator from being damaged.

With regard to Claim 14, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit according to claim 13, wherein said second switch is a transistor.

With regard to Claim 15, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit according to claim 13, wherein: the second switch is configured to periodically energize the coil-armature device according to the first duty cycle for a determined period of time sufficient to move the armature to a center of the coil, and the second

switch is configured to periodically energize the coil-armature device according to the second duty cycle subsequent to the period of time sufficient to move the armature to the center of the coil (column 1 lines 62-67 & column 2 lines 1-9).

With regard to Claim 16, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit according to claim 13, further comprising a first comparator (60) configured to generate a control signal in response to a comparison between a voltage signal indicative of an amount of energy stored in said coil-armature device and a first reference signal (column 4 lines 61-67 & column 5 lines 1-31).

With regard to Claim 17, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit of claim 16, wherein said voltage signal indicative of an amount of energy stored in said coil-armature device is generated across a resistor (R16) connected in series with the coil-armature device (20).

With regard to Claim 18, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit of claim 16, wherein: the first reference signal has a first voltage level during a time period sufficient to move the armature to a center of the coil, and said first reference signal has a second voltage level subsequent to said time period sufficient to move the armature to the center of the coil (column 5 lines 32-48).

With regard to Claims 19-21, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit of claim 16, wherein said first reference signal is generated from a voltage divider circuit, wherein said voltage divider circuit is adjustable so as to be able to change said first reference signal in response to a circuit mode signal, wherein the voltage divider comprises a plurality of resistors (R12-R14), and wherein at least one of the resistors (R12) is configured to be electrically shorted from said voltage divider in response to a circuit mode signal (column 5 lines 32-48).

With regard to Claims 22-24, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit of claim 21, further comprising a second comparator (56) that compares a second input signal to a second reference signal to generate said circuit mode signal, wherein said second input signal is generated based on a voltage level across a capacitor (C5), wherein said capacitor is sized so that said second input signal exceeds said second reference signal after a determined time sufficient to move the armature to a center of the coil has elapsed (column 5 lines 32-48).

With regard to Claim 25, Hansen et al. in view of Sasaki, in Figure 2, discloses the circuit of claim 22, wherein the second input signal is configured to exceed said second reference signal after a determined time sufficient to move the armature to a center of the coil has elapsed (column 5 lines 32-48).

With regard to Claim 26, Hansen et al. in view of Sasaki, in Figure 2 teaches the circuit according to claim 16.

Hansen et al. does not teach a relay positioned between the first comparator and the second switch.

Hansen et al., does however teach that a transistor (Q3) is positioned between the first comparator (60) and the second switch (Q2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a relay instead of a transistor as the two are art recognized functional equivalents of each other, A relay is used instead of a transistor for the purpose of allowing the switch to draw more current and to eliminate capacitance in the circuit that would slow circuit operation.

5. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen et al. in view of Sasaki as applied to claim 16 above and further in view of Bartsch (US 5,687,050).

With regard to Claim 35, Hansen et al. in view of Sasaki, teaches the circuit of claim 16.

Hansen et al. in view of Sasaki, does not teach a feedback capacitor connected in parallel to said first comparator and configured to prevent the interference of random oscillations generated by the operation of the first comparator.

Bartsch, in Figure 2, teaches a circuit to control a solenoid wherein a feedback capacitor is providing in parallel to a comparator.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hansen et al. in view of Sasaki, with

Bartsch, by placing a feedback capacitor in parallel with the first comparator of Hansen et al., for the purpose of filtering noise (Bartsch column 3 lines 54-56).

Allowable Subject Matter

Claim 36 is allowable because it was rewritten in independent form including all of the limitations of the base claim and all intervening claims. Reasons for Allowance were given in the previous actions.

Response to Arguments

Applicant's arguments filed 11 JAN 2007 have been fully considered but they are not persuasive. Applicant initially argues that neither Stoll, Yoshimura nor Briedis teach a pulse width modulation signal generator including an inverter and a feedback Loop. Pulse width modulation can be defined as the modulation of a duty cycle, to either convey information over a communications channel or control the amount of power sent to a load. Stoll in column 8 lines 17-20 teaches that the oscillation generator creates pulses to cause a transistor to be turned on and off such that the initially high attraction force will be redeuced to a low holding current. While Stoll does not directly state that the oscilation generator provides PWM, the circuit modulates a duty cyle to control the amount of power sent to a load. Stoll however, employs a different method of creating an oscillating signal than claim 1. The Yoshimura reference was then relied upon to teach an improved method of generating an oscillation for th PWM of Stoll et al. As such, Stoll et al. in view of Yoshimura teaches all the features of claim.

Which regard to Applicant's argument that Hansen in view of Sasaki does not teach or suggest an analog switch responsive to a change mode, that causes a transition from said first duty cycle to said second duty cycle, one cannot show, nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Hansen teaches that a comparator (56) outputs a change mode signal that causes a transition from a first duty cycle to a second duty cycle. The only element that Hansen does not teach is an analog switch that is responsive to the change mode signal already provided by Hansen. As Sasaki teaches that an analog switch can be coupled between an output of a comparator and other circuit components the two references are analogous art. As stated on page 8 lines 8-14 of the previous Office Action, when combined, the references would necessarily teach that an analog switch, placed after the comparator in the circuit of Hansen causes a transition from a first duty cycle to a second duty cycle. When combined the two references teach all the language of claim 13. Additional language describing the specific placement of the analog switch in the circuit would help differentiate the circuit of Hansen in view of Sasaki from the present invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAB
02 APR 2007

Stephen W. Jackson
4-2-07

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